Notice of Allowability	Application No.	Applicant(s)	
	09/850,237	LEE ET AL.	
	Examiner	Art Unit	
	Grigory Gurshman	2132	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address--

All claims being allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included herewith (or previously mailed), a Notice of Allowance (PTOL-85) or other appropriate communication will be mailed in due course. **THIS NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RIGHTS.** This application is subject to withdrawal from issue at the initiative of the Office or upon petition by the applicant. See 37 CFR 1.313 and MPEP 1308.

1. ☒ This communication is responsive to *Terminal Disclaimer filed on 1/31/2005*.

2. ☒ The allowed claim(s) is/are *1-65*.

3. ☐ The drawings filed on _____ are accepted by the Examiner.

4. ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
   a) ☐ All b) ☐ Some* c) ☐ None of the:
      1. ☐ Certified copies of the priority documents have been received.
      2. ☐ Certified copies of the priority documents have been received in Application No. _____ .
      3. ☐ Copies of the certified copies of the priority documents have been received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

   * Certified copies not received: _____.

Applicant has THREE MONTHS FROM THE "MAILING DATE" of this communication to file a reply complying with the requirements noted below. Failure to timely comply will result in ABANDONMENT of this application.
THIS THREE-MONTH PERIOD IS NOT EXTENDABLE.

5. ☐ A SUBSTITUTE OATH OR DECLARATION must be submitted. Note the attached EXAMINER'S AMENDMENT or NOTICE OF INFORMAL PATENT APPLICATION (PTO-152) which gives reason(s) why the oath or declaration is deficient.

6. ☒ CORRECTED DRAWINGS (as "replacement sheets") must be submitted.
   (a) ☐ including changes required by the Notice of Draftsperson's Patent Drawing Review (PTO-948) attached
      1) ☐ hereto or 2) ☐ to Paper No./Mail Date _____.
   (b) ☒ including changes required by the attached Examiner's Amendment / Comment or in the Office action of Paper No./Mail Date 2/15/2005.

   Identifying indicia such as the application number (see 37 CFR 1.84(c)) should be written on the drawings in the front (not the back) of each sheet. Replacement sheet(s) should be labeled as such in the header according to 37 CFR 1.121(d).

7. ☐ DEPOSIT OF and/or INFORMATION about the deposit of BIOLOGICAL MATERIAL must be submitted. Note the attached Examiner's comment regarding REQUIREMENT FOR THE DEPOSIT OF BIOLOGICAL MATERIAL.

Attachment(s)

1. ☒ Notice of References Cited (PTO-892)
2. ☐ Notice of Draftperson's Patent Drawing Review (PTO-948)
3. ☐ Information Disclosure Statements (PTO-1449 or PTO/SB/08), Paper No./Mail Date _____
4. ☐ Examiner's Comment Regarding Requirement for Deposit of Biological Material
5. ☐ Notice of Informal Patent Application (PTO-152)
6. ☐ Interview Summary (PTO-413), Paper No./Mail Date _____ .
7. ☐ Examiner's Amendment/Comment
8. ☒ Examiner's Statement of Reasons for Allowance
9. ☐ Other _____.

DETAILED ACTION

Drawings

1. The drawings filed on 5/07/2001 are acceptable subject to minor correction of the informalities consisting of hand written text in Figs. 4A and 6. In order to avoid abandonment of this application, correction is required. The correction will not be held in abeyance.

2. ***Double Patenting***

The double patenting rejection based on the provisional non-statutory double patenting has been overcome by a the Terminal Disclaimer filed on 1/31/2005.

Allowable Subject Matter

3. Claims 1-65 are allowed.

4. The following is an examiner's statement of reasons for allowance:

4.1 The following prior art was found in process of searching for the claimed invention:

U.S. Patent No. 6.446.198 B1 to Sazegari ;

U.S. Patent No. 6.629.115 B1 to Rossignol ;

U.S. Patent No. 6.381.690 B1 to Lee ;

U.S. Patent No. 5.546.393 to Minc ;

U.S. Patent No. 5.495.476 to Kumar

4.2 Referring to the independent claims 1, 15, 17, 21, 24, 38, 40, 41, 44, 46, 49, 52, 55 ,58, 59, 62, 63,64 and 65, Sazegari discloses a vectorized table lookup. Sazegari teaches sets of data consisting of two vectors, which constitute the operands for a permute instruction. Only a limited number of bits are required to index into the table during the execution of this instruction. The remaining bits of each index are used as masks into a series of select instructions. The select instruction chooses between two vector components, based on the mask, and places the selected components into a new vector. The mask is generated by shifting one of the higher order bits of the index to the most significant position, and then propagating that bit throughout a byte, for example by means of an arithmetic shift. This procedure is carried out for all of the index bytes in the vector, to generate a select mask. The select mask is then used during a select operation, to choose between the results of permute instructions on different ones of the logically divided sets of data (see abstract and Figs 3-6).

4.3 Referring to the instant claims, Kumar discloses a parallel algorithm to set up benes switch. Kumar teaches a method for handling dynamically varying communication patterns efficiently by operating the Benes network in a time division multiplexed manner, wherein during a given transmission period, the middle stage switches of the Benes network are configured as a portion of the middle stage switches of a Clos network configured to route all signals in a single period (see abstract and Figs. 2-4).

4.4 Referring to the instant claims, Lee discloses a processor for performing subword permutations and combinations. Lee teaches an apparatus for operating on the

contents of an input register to generate the contents of an output register which contains a permutation, with or without repetitions, or a combination of the contents of the input register. The apparatus partitions the input register into a plurality of sub-words, each sub-word being characterized by a location in the input register and a length greater than one bit. In response to an instruction specifying a rearrangement of the input register, the present invention directs at least one of the sub-words in the input register to a location in the output register that differs from the location occupied by the sub-word in the input register (see abstract and Figs. 2-3).

4.5 Referring to the instant claims, Minc discloses an asynchronous transfer mode data cell routing device for a reverse omega network. Minc teaches a routing bits generator is associated with one or more reverse Omega networks with L stages and 2.sup.N inputs. 2.sup.N state bits, indicating whether the cells to be routed are free or occupied, are loaded in parallel into a state register, then shifted in series in this register. The state bits delivered successively by the serial output of the state register, filtered if L<N, serve to increment a first counter or decrement a second counter depending on the values of the state bits, and to select one or the other of the two counters at the input of a multiplexer. L addressing registers, receiving in serial shift mode the L address bits provided by the multiplexer, are cascaded in such a way that after 2.sup.N serial shift cycles, their contents can be transferred in parallel to means inserting the address bits at the head of the cells (see abstract and Figs. 6-11).

4.6 Referring to the instant claims, Rossignol discloses a method and apparatus for manipulating vectored data. Rossignol teaches a method and apparatus is disclosed for

manipulating vectored data. The method includes shifting bits of packed data comprising M N-bit elements using a bit-level shift step followed by a byte-level shift step. A mask is generated and applied to the intermediate shifted result to produce the final result. A method is disclosed for conditionally transferring data from one general purpose register to another based on data in yet a third general purpose register (see abstract and Fig. 4-7, 9-11).

4.7 Neither one of the above cited references teach or suggest the following:

a. defining an intermediate sequence of bits that said source sequence of bits is transformed into;

b. determining a permutation instruction for transforming said source sequence of bits into said intermediate sequence of bits; and

c. repeating steps a. and b. using said determined intermediate sequence of bits from step b. as said source sequence of bits in step a. until a desired sequence of bits is obtained, wherein the determined permutation instructions form a permutation instruction sequence.

Further more, prior art does not teach performing steps a-c based on configuration of Benes network.

Further more none of the prior art of record teaches or suggests performing the permutations in a processor by performing the steps a – g:

" a. dividing bits of a first of the source registers to be placed in a first destination

register into a first group and bits of said first of said source registers to be placed in a second destination register into a second group with a first permutation instruction sequence,

b. dividing bits of a second of the source registers to be placed in said first destination register into a first group and bits of the second of the source registers to be placed in a second destination register into a second group with a second permutation instruction sequence,

c. placing bits of said first group of said first of said source registers and said bits of said first group of said second of said source registers into said first destination register;

d. placing bits of said second group of said first of said source registers and said second group of said second of said registers into said second destination register;

e. defining a sequence of bits of said first destination register as a first source sequence of bits and a sequence of bits of said second destination register as a second source sequence of bits; identifying an intermediate sequence of bits that each of said first source sequence of bits and said second source sequence of bits is transformed into;

g. determining a permutation instruction for transforming said first source sequence of bits and said second source sequence of bits into respective said intermediate sequence of bits; and repeating steps f. and g. using said determined intermediate sequence of bits from step g. as said source sequence of bits in step f. untill a respective desired sequence of bits is obtained for said first source sequence of bits and said second source sequence of bits, wherein the determined permutation

instructions form a permutation instruction sequence. " , recited in the independent claims 17 and 38.

5. Claims 1-65 are in condition for allowance in view of reason stated herein.

Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Grigory Gurshman whose telephone number is (571)272-3803. The examiner can normally be reached on 9 AM-5:30 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Gilberto Barron can be reached on (571)272-3799. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

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